**Final Project Proposal: Optimized High Speed and Low Power Multiplier**

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# Introduction

Multiplication is a critical and unavoidable operation in most of the real-world systems. However, multipliers usually take many cycles to generate outputs, thus may not be able to deliver data to the next computation stage in a timely manner. In addition, long latency combinational logic leads to relatively low throughput. Latency issue apart, area complexity is also a concern in modern designs such that the multiplier should be compact, otherwise may induce potentially more power dissipation and higher financial cost. Therefore, we are motivated to propose a new multiplier solution by using pipelined structure, modified Booth encoding, fast sign-extension method, and a better summation architecture with advanced adder. Specifically, we aims to optimize the multiplier targeting at lower delay, higher throughput, and relatively lower area complexity.

# Background

Booth multiplier [1], is based on an algorithm designed for fast multiplication. It first re-encodes adjacent bits in one of the multiplicand, aimed at reducing the number of partial products. Then all the partial products will be simply calculated and sign-extended in order to achieve multiplication of two’s complement numbers. Finally, weighted summation will be applied to those partial products to generate the result. Therefore, there are several issues for us to address: (1) how to trade-off between performance benefit and overhead of different radix of Booth algorithm; (2) how to achieve efficient sign extension; (3) how to achieve higher performance in partial product summation; and (4) how to reduce the area complexity of the hardware design.

To address the above issues, a number of algorithms and methodologies have been proposed in the literature. Particularly, S. Abraham *et al*. [2] proposes a modified Booth multiplier that halves the number of partial products. S. Dubey *et al*. [3] shows a Wallace Tree multiplier where the partial products are computed by Booth multiplier, and this architecture innovation results in significant reduction in delay. R. D. Kshirsagar *et al*. [4] demonstrates a Wallace-tree-based high throughput multiplier by using a four-stage pipeline.

# Method

Specifically, we first partition the whole multiplier into 3 pipeline stages, with the first stage being Booth encoding, the second being partial product generation with sign extension, and the third being partial product summation. For encoding and partial product generation, we adopted radix-4 modified Booth algorithm to re-encode one of the multiplicand and generate reduced partial products. Then we adopt the Reduced Area (RA) Reduction to perform fast summation. Lastly, instead of using full adders and half adders, we will incorporate LING adders [5] in our design to reduce critical path latency. Note that the final summation will be achieved by a simple Carry Look-ahead Adder (CLA).

To evaluate our design, we will first start with theoretical analysis of it in terms of delay and complexity. Second, we will validate the functionality of our design by functional simulation. Then we will compare our design with other summation architectures, such as Wallace tree and Dadda tree. Then we compare the timing between pipelined multiplier and non-pipelined one to show the throughput augmentation of our proposed design. Finally, in order to validate the effectiveness of LING adder, we also conduct comparison experiment with other widely used adders, such as Carry Select Adder (CSA), and 5-3 Counter. Through these exploitation, we may find a better optimized multiplier solution.

# Reference

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